Concordia University

Laboratory Report

COEN - 316

Experiment – 1

ALU

Submission Date: October 10, 2019

Prepared by

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Name Student ID

“I certify that this submission is my original work and meets the Faculty's Expectations of Originality”

* ModelSim Simulation of ALU: (please zoom in the figures if required)

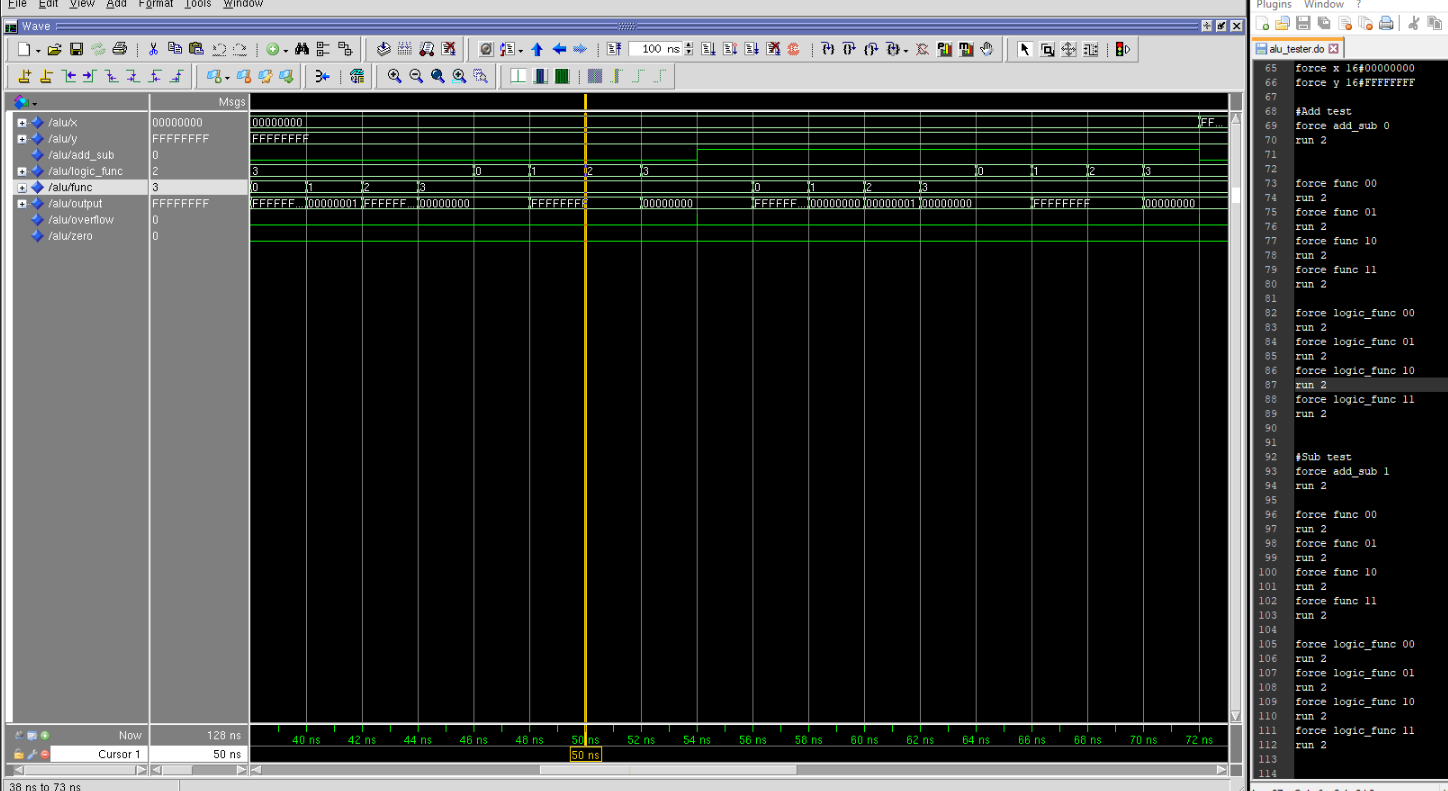


Figure Simulation of arithmetic and logical operation of the ALU, with the values of X = x00000000 (hex) and Y = xFFFFFFFF (hex); Duration 38 to 72ns; A snapshot of the do file is shown on the right

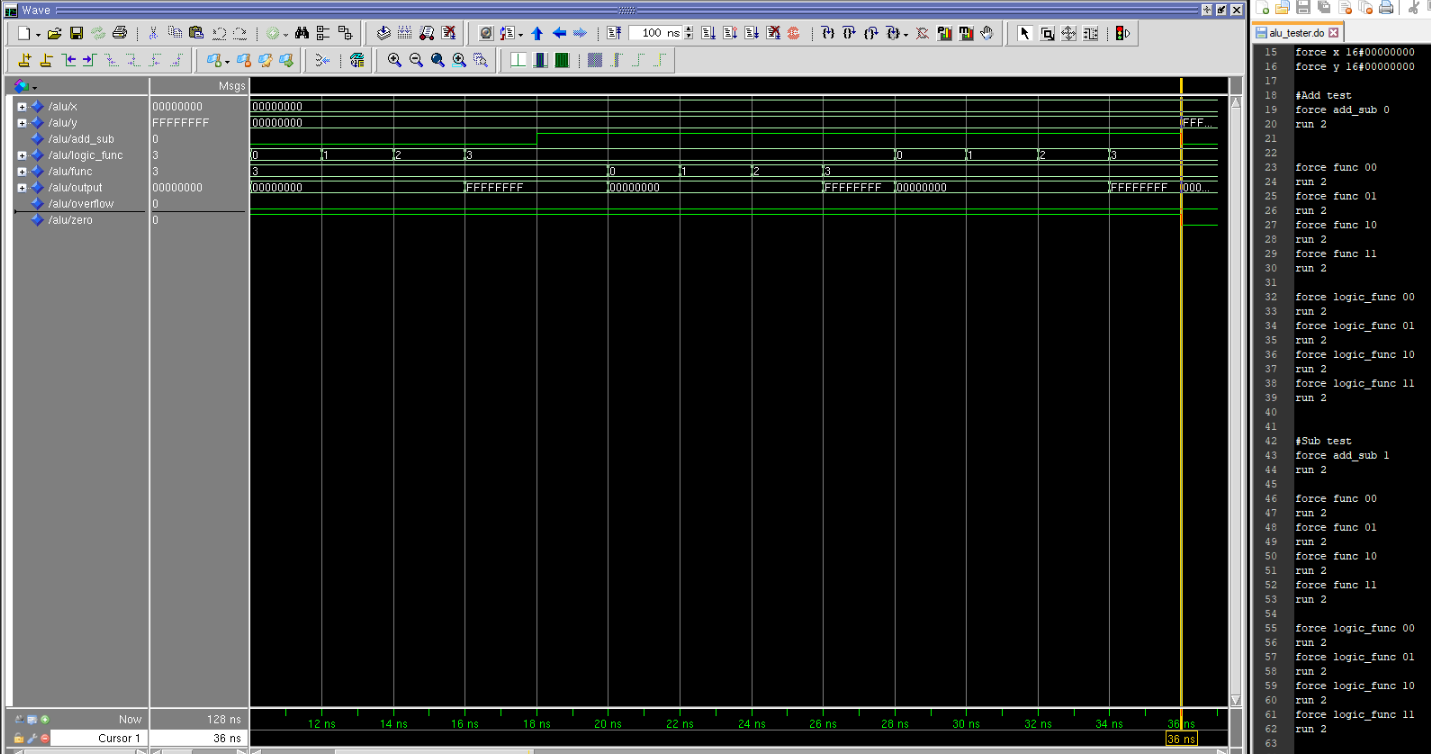


Figure Simulation of arithmetic and logical operation of the ALU, with the values of X = x00000000 (hex) and Y = x00000000 (hex); Duration 10 to 36ns; A snapshot of the do file is shown on the right

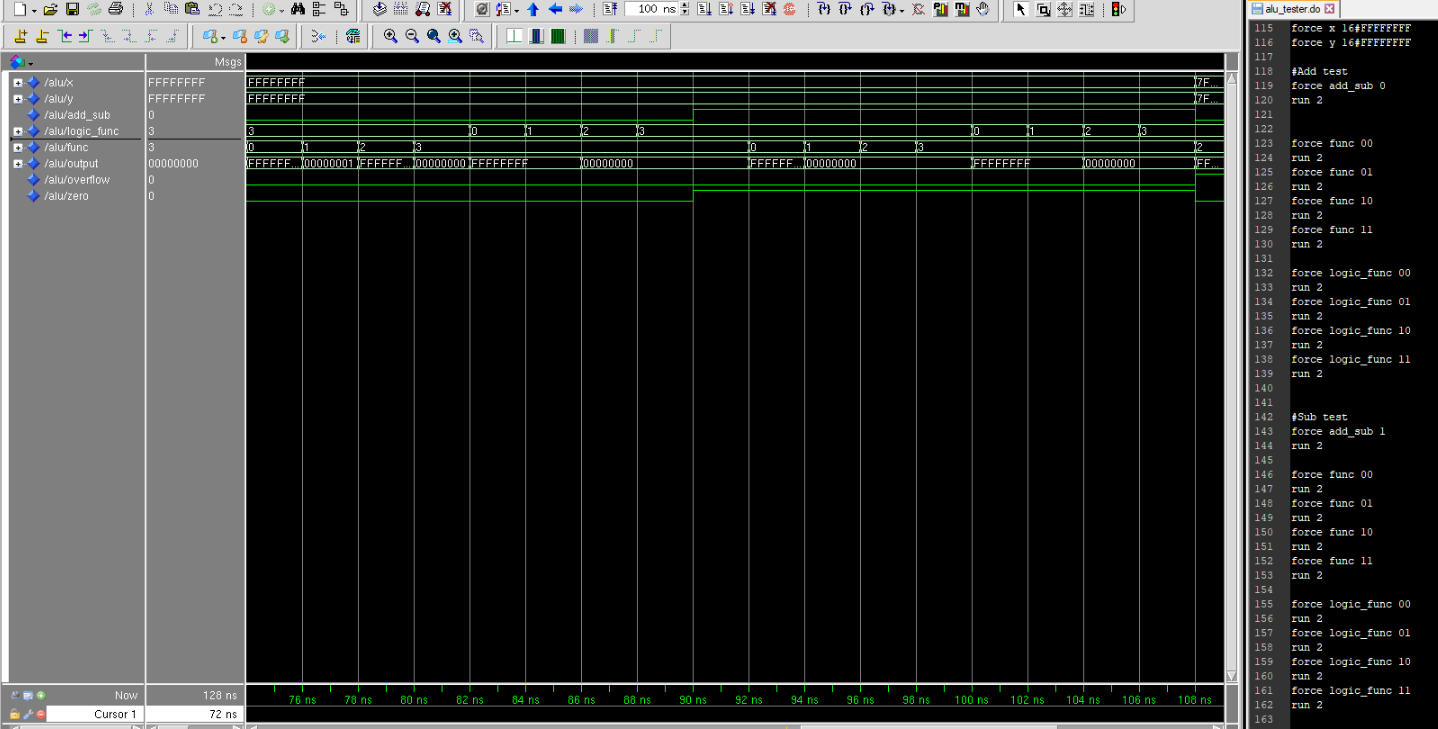


Figure Simulation of arithmetic and logical operation of the ALU, with the values of X = xFFFFFFFF (hex) and Y = xFFFFFFFF (hex); Duration 72 to 108ns; A snapshot of the do file is shown on the right

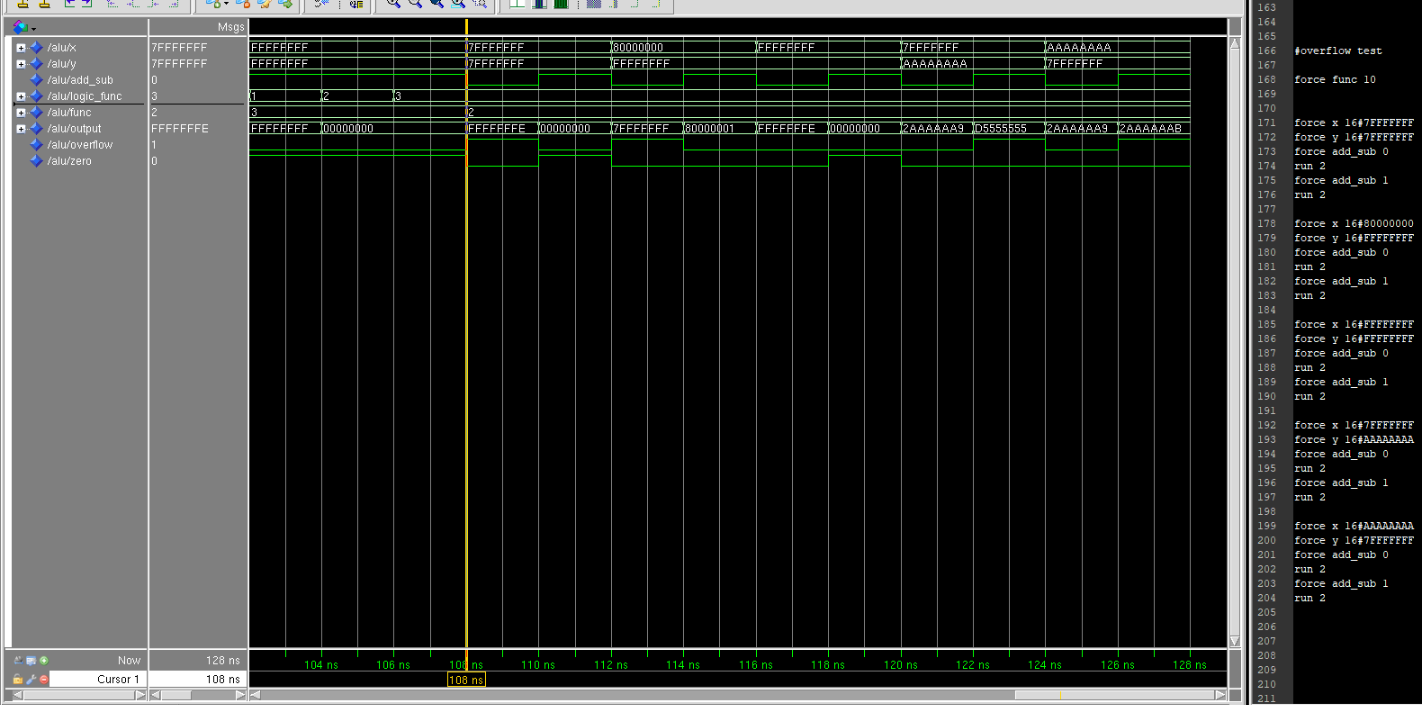


Figure Simulation of overflow based on different values of X and Y

* Precision log file

# Info: [9566]: Logging project transcript to file /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1\_impl\_1/precision.log

# Info: [9566]: Logging suppressed messages transcript to file /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1\_impl\_1/precision.log.suppressed

# Info: [9550]: Activated implementation lab1\_impl\_1 in project /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1.psp.

new\_project -name lab1 -folder /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1 -createimpl\_name lab1\_impl\_1

# COMMAND: add\_input\_file {../../32-bit-CPU/alu.vhd}

add\_input\_file {../../32-bit-CPU/alu.vhd}

# COMMAND: setup\_design -manufacturer Xilinx -family "VIRTEX-II Pro" -part 2VP30ff896 -speed -7

# Info: [15298]: Setting up the design to use synthesis library "xcv2p.syn"

# Info: [575]: The global max fanout is currently set to 10000 for Xilinx - VIRTEX-II Pro.

# Info: [15324]: Setting Part to: "2VP30ff896".

# Info: [15325]: Setting Process to: "7".

# Info: [7512]: The place and route tool for current technology is ISE.

setup\_design -manufacturer Xilinx -family "VIRTEX-II Pro" -part 2VP30ff896 -speed -7

# COMMAND: setup\_design -frequency 100 -max\_fanout=10000

# Info: [575]: The global max fanout is currently set to 10000 for Xilinx - VIRTEX-II Pro.

setup\_design -frequency 100 -max\_fanout=10000

# COMMAND: compile

# Info: [3022]: Reading file: /CMC/tools/mentor/precision/Mgc\_home/pkgs/psr/techlibs/xcv2p.syn.

# Info: [634]: Loading library initialization file /CMC/tools/mentor/precision/Mgc\_home/pkgs/psr/userware/xilinx\_rename.tcl

# Info: XILINX

# Info: [40000]: vhdlorder, Release 2016a.7

# Info: [40000]: Files sorted successfully.

# Info: [40000]: hdl-analyze, Release RTLC-Precision 2016a.7

# Info: [42502]: Analyzing input file "/nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/../../32-bit-CPU/alu.vhd" ...

# Error: [42996]: "/nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/../../32-bit-CPU/alu.vhd", line 135: Illegal reference of signal - cannot elaborate statically

# Error: [40008]: HDL analysis failed.

compile

# COMMAND: exit -force

# Warning: [9526]: Discarded unsaved work in implementation lab1\_impl\_1.

# Info: [9565]: Appending project transcript to file /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1\_impl\_1/precision.log

# Info: [9565]: Appending suppressed messages transcript to file /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1\_impl\_1/precision.log.suppressed

# Info: [9550]: Activated implementation lab1\_impl\_1 in project /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1.psp.

open\_project /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1.psp

# COMMAND: add\_input\_file {../../32-bit-CPU/alu.vhd}

add\_input\_file {../../32-bit-CPU/alu.vhd}

# COMMAND: setup\_design -manufacturer Xilinx -family "VIRTEX-II Pro" -part 2VP30ff896 -speed -7

# Info: [15298]: Setting up the design to use synthesis library "xcv2p.syn"

# Info: [575]: The global max fanout is currently set to 10000 for Xilinx - VIRTEX-II Pro.

# Info: [15324]: Setting Part to: "2VP30ff896".

# Info: [15325]: Setting Process to: "7".

# Info: [7512]: The place and route tool for current technology is ISE.

setup\_design -manufacturer Xilinx -family "VIRTEX-II Pro" -part 2VP30ff896 -speed -7

# COMMAND: setup\_design -frequency 100 -max\_fanout=10000

# Info: [575]: The global max fanout is currently set to 10000 for Xilinx - VIRTEX-II Pro.

setup\_design -frequency 100 -max\_fanout=10000

# COMMAND: compile

# Info: [3022]: Reading file: /CMC/tools/mentor/precision/Mgc\_home/pkgs/psr/techlibs/xcv2p.syn.

# Info: [634]: Loading library initialization file /CMC/tools/mentor/precision/Mgc\_home/pkgs/psr/userware/xilinx\_rename.tcl

# Info: XILINX

# Info: [40000]: vhdlorder, Release 2016a.7

# Info: [40000]: Files sorted successfully.

# Info: [40000]: hdl-analyze, Release RTLC-Precision 2016a.7

# Info: [42502]: Analyzing input file "/nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/../../32-bit-CPU/alu.vhd" ...

# Info: [659]: Top module of the design is set to: alu.

# Info: [657]: Current working directory: /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1\_impl\_1.

# Info: [40000]: RTLC-Driver, Release RTLC-Precision 2016a.7

# Info: [40000]: Last compiled on Jun 2 2016 06:11:46

# Info: [44512]: Initializing...

# Info: [44504]: Partitioning design ....

# Info: [40000]: RTLCompiler, Release RTLC-Precision 2016a.7

# Info: [40000]: Last compiled on Jun 2 2016 06:47:43

# Info: [44512]: Initializing...

# Info: [44522]: Root Module work.alu(alu\_architecture): Pre-processing...

# Info: [44523]: Root Module work.alu(alu\_architecture): Compiling...

# Info: [44842]: Compilation successfully completed.

# Info: [44856]: Total lines of RTL compiled: 149.

# Info: [44835]: Total CPU time for compilation: 0.0 secs.

# Info: [44513]: Overall running time for compilation: 5.0 secs.

# Info: [657]: Current working directory: /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1\_impl\_1.

# Info: [15330]: Doing rtl optimizations.

# Info: [660]: Finished compiling design.

compile

# COMMAND: synthesize

# Info: [657]: Current working directory: /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1\_impl\_1.

# Info: [15002]: Optimizing design view:.work.alu.alu\_architecture

# Info: [3027]: Writing file: /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1\_impl\_1/alu.edf.

# Info: [3027]: Writing file: /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1\_impl\_1/alu.ucf.

# Info: [660]: Finished synthesizing design.

# Info: [11019]: Total CPU time for synthesis: 0.9 s secs.

# Info: [11020]: Overall running time for synthesis: 1.2 s secs.

synthesize

# COMMAND: save\_project

# Info: [9562]: Saved implementation lab1\_impl\_1 in project /nfs/home/s/sal\_rahm/316/fpga\_adv/lab1/lab1.psp.

save\_project

* RTL schematic and Tech schematic

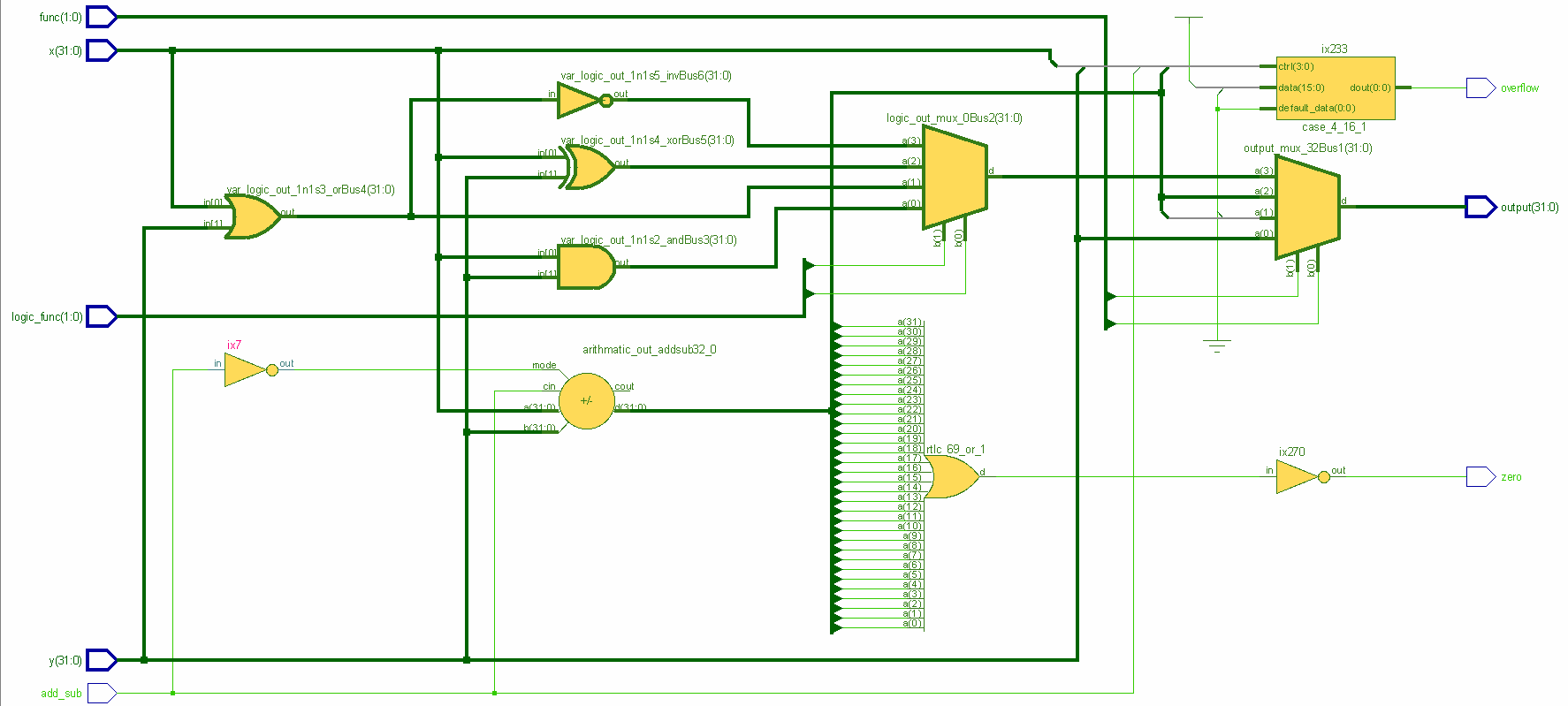


Figure RTL schematic of the vhdl code

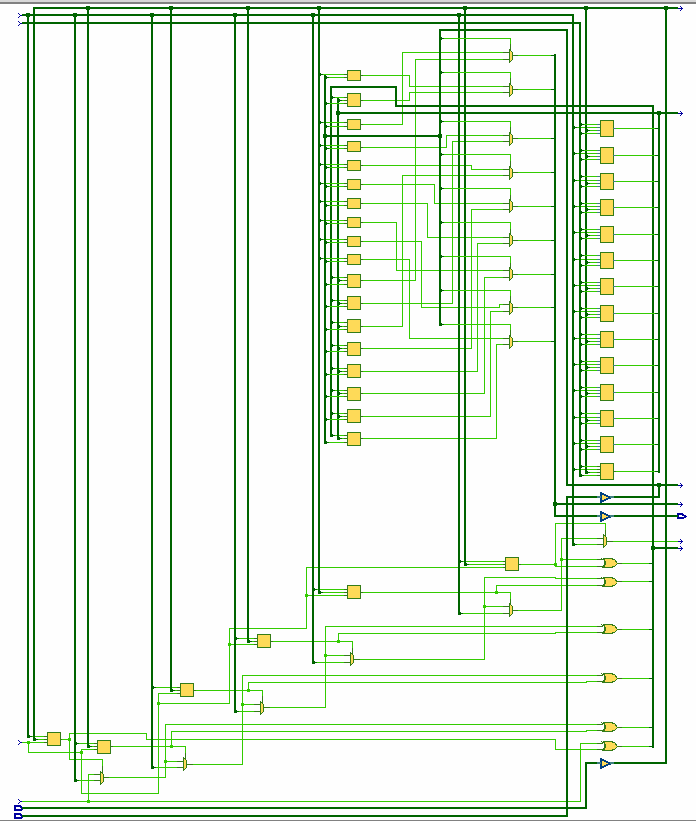


Figure Tech schematic of the synthesis

* ALU.UCF file

# Precision RTL Synthesis 64-bit 2016.1.0.15 (Production Release) Wed Jun 8 09:35:56 PDT 2016

CONFIG STEPPING="0";

NET output(0) LOC = T6;

NET output(1) LOC = V1;

NET output(2) LOC = R3;

NET output(3) LOC = R5;

NET output(4) LOC = T2;

NET output(5) LOC = P4;

NET output(6) LOC = R7;

NET output(7) LOC = P2;